MULTI-FINGER TYPE ELECTROSTATIC DISCHARGE PROTECTION CIRCUIT

RELATED APPLICATION

[01] The present application claims the benefit of Korean Patent Application No. 87295/2000 filed December 30, 2000, under 35 U.S.C. § 119, which is herein fully incorporated by reference.

BACKGROUND OF THE INVENTION

Field of the Invention

[02] The present invention relates to an electrostatic discharge protection circuit, and more particularly, to a multi-finger type electrostatic discharge protection circuit.

Background of the Related Art

[03] Electrostatic discharge (ESD) characteristics of a device generally depend on whether or not the MOS

transistors of an ESD protection circuit properly allow the discharge of ESD pulses. A general ESD protection circuit has a multi-finger structure in which a plurality of gates are arranged consecutively in a single active area so as to discharge the ESD pulses.

[04] Fig. 1 illustrates a layout of a multi-finger type ESD protection circuit according to a related art.

[05] Referring to Fig. 1, in this multi-finger type ESD protection circuit having NMOS transistors, a plurality of gates (gate fingers) 103 are arranged in a large active region 100 side by side in a multi-finger configuration. A n+ type source region 101 and a n+ type drain region 102 are symmetrically arranged on both sides of each gate 103 to form NMOS type transistors. Contacts 104 and a p+ type active region 105 for bulk (substrate) bias are provided around the active region 100.

[06] Generally, the drain region 102 is connected to an input or output pad, and the source and active regions 101 and 105 are connected to a ground Vss. The gates 103

are also connected to the ground Vss. If the NMOS transistor is used as a pull-down transistor, the gate 103 is connected to an output of a pull-down inverter as known in the art.

[07] The npn bipolar operation between an n+ junction of the source region 101 and the other n+ junction of the adjacent drain region 102 discharges, as known, a positive ESD pulse having been applied thereto through an input/output pad as a Vcc reference voltage. A negative ESD pulse having been applied thereto through an input/output pad as a Vcc reference voltage is discharged by the forward npn bipolar operation between an n+ junction of the drain region 102 and the p+ junction of the active region 105.

[08] Fig. 2 is a functional diagram of the ESD protection circuit having the multi-finger type NMOS transistors as shown in Fig. 1.

[09] As mentioned in the above explanation, in Fig. 2, if a Vcc reference voltage is applied to a particular

input/output pad 11 connected to the drain regions, the corresponding NMOS transistor 10 discharges an ESD pulse by an npn bipolar operation between n+ junctions of the source and drain regions of the corresponding NMOS transistor 10.

[10] However, it may happen that portions of the gate fingers are not turned on in a conventional multi-finger type NMOS transistor structure when an ESD pulse is applied thereto. As a result, npn bipolar operations are not carried out uniformly in all the gate fingers. But, the parasitic npn bipolar operation occurs locally in some of the gate fingers. Thus, the other gate fingers fail to perform the parasitic npn bipolar operation. Such a phenomenon worsens as the number of multi-finger type transistors increases, whereby the ESD protection circuit according to the related art fails to carry out the ESD protection function as designed.

[11] Further, a Vcc reference ESD pulse having been applied thereto through an input/output pad as a Vcc

reference is discharged by a forward npn bipolar operation between the n+ junction of the drain region and the p+ junction of the active region. Yet, all of the n+ junctions of the drain regions in the conventional multi-finger type NMOS transistor structures fail to have uniform resistance against the p+ junction of the active region, whereby the ESD pulse discharge performance of the ESD protection circuit according to the related art is weak and needs improvement.

SUMMARY OF THE INVENTION

[12] Accordingly, the present invention is directed to a multi-finger type electrostatic discharge protection circuit/device that substantially obviates one or more problems due to limitations and disadvantages of the related art.

[13] An object of the present invention is to provide a multi-finger type electrostatic discharge protection circuit/device with improved ESD protection performance

and characteristics.

[14] Additional advantages, objects, and features of the invention will be set forth in part in the description which follows and in part will become apparent to those having ordinary skill in the art upon examination of the following or may be learned from practice of the invention. The objectives and other advantages of the invention may be realized and attained by the structure particularly pointed out in the written description and claims hereof as well as the appended drawings.

[15] To achieve these objects and other advantages and in accordance with the purpose of the invention, as embodied and broadly described herein, a multi-finger type electrostatic discharge protection circuit according to an embodiment of the present invention includes a semiconductor substrate, a plurality of active regions formed separately on the semiconductor substrate, and a pair of gates formed on each of the respective active regions. Preferably, the present invention discharges an

ESD pulse effectively by forming additional n+ (or p+) type active regions, which are connected to Vcc (or Vss), between the respective active regions.

[16] In another aspect of the present invention, a multi-finger type electrostatic discharge protection circuit includes a semiconductor substrate, a plurality of active regions formed separately on the semiconductor substrate, a pair of gates formed on each of the respective active regions, and predetermined conductive type active regions formed between the respective active regions.

[17] In a further aspect of the present invention, a multi-finger type electrostatic discharge protection circuit includes a semiconductor substrate, a plurality of active regions formed separately on the semiconductor substrate, a pair of gates formed on each of the respective active regions, drain regions formed at n+ junctions of both ends of the respective active regions, source regions formed between the two gates of the

respective active regions, and predetermined conductive type active regions formed between the respective active regions.

[18] It is to be understood that both the foregoing general description and the following detailed description of the present invention are exemplary and explanatory and are intended to provide further explanation of the invention as claimed.

BRIEF DESCRIPTION OF THE DRAWINGS

[19] The accompanying drawings, which are included to provide a further understanding of the invention and are incorporated in and constitute a part of this application, illustrate embodiment(s) of the invention and together with the description serve to explain the principle of the invention. In the drawings;

[20] Fig. 1 illustrates a layout of a multi-finger type ESD protection circuit according to a related art;

[21] Fig. 2 illustrates a functional diagram of a

portion of the ESD protection circuit in Fig. 1 according to a related art;

[22] Fig. 3 illustrates a layout of a multi-finger type ESD protection circuit according to an embodiment of the present invention; and

[23] Fig. 4 illustrates a functional diagram of a portion of the ESD protection circuit in Fig. 3 according to the present invention.

DETAILED DESCRIPTION OF THE PREFERRED EMBODIMENTS

[24] Reference will now be made in detail to the preferred embodiments of the present invention, examples of which are illustrated in the accompanying drawings.

[25] Fig. 3 illustrates a layout of a multi-finger type ESD protection circuit according to an embodiment of the present invention.

[26] Referring to Fig. 3, in an ESD protection circuit according to the present invention, a plurality of active regions 200 are provided. For each active region

.200, a pair of gates 203 and 204 are formed in the active region 200, a pair of drain regions 202 and 205 are formed at an n+ junction of both ends of the active region 200, and a source region 206 is formed at the n+ junction between the gates 203 and 204 to form multi-finger type NMOS transistors. A separated, predetermined type (n+ or p+) active region 201 is arranged between two adjacent active regions 200. Moreover, a p+ type active region 207 as a guard ring and contacts 210 are formed at a circumference of the multi-finger type NMOS transistors, which is identical to the features of the related art.

SUB A1

[27] For each active region 200, the drain regions 202 and 205 are connected to an input or output pad, the source region 206 is connected to a ground Vss, and the pair of the gates 203 and 204 are connected to the ground Vss or an output of a pull-down inverter when used as a pull-down transistor. The n+ active region 201 between two active regions 200 is connected to Vcc (or Vss when the active region 201 is of p+ type).

[28] The electrostatic discharging operation of the ESD protection circuit according to the present invention for different scenarios is now described by referring to Figs. 3 and 4.

[29] Scenario (1): when the active region 201 of n+ type is formed between two adjacent active regions 200.

[30] In this scenario, if a positive ESD pulse (e.g., as a Vcc reference voltage) is applied thereto through an input/output pad 21 connected the multi-finger transistors, the applied ESD pulse is effectively discharged by an npn bipolar operation occurring between the n+ junctions of the drain and source regions 202 and 206 of the active region 200 as well as by a parasitic npn bipolar operation occurring between the drain region 205 and the n+ active region 201.

[31] If a negative ESD pulse is applied thereto through the input/output pad 21, an np diode operation occurring between the n+ junction of the drain region 202 and the p+ junction of the active region 207 effectively

discharges the applied ESD pulse.

[32] Scenario (2): when the active region 201 of p+ type is formed between two active regions 200.

[33] In this scenario, if a positive ESD pulse is applied thereto through an input/output pad 21, the applied ESD pulse is effectively discharged by an npn bipolar operation occurring between the n+ junctions of the drain and source regions 202 and 206.

[34] If a negative ESD pulse is applied thereto through the input/output pad 21, the negative ESD pulse is effectively discharged by an np diode operation occurring between the n+ junction of the drain region 202 and the p+ junction of the active region 207 as well as a forward npn diode operation occurring between the drain region 202 and the p+ active region 201.

[35] As mentioned in the above description, the NMOS type ESD protection circuit of the present invention is designed such that a pair of gates are formed in parallel with each other in a single active region to enable all

the gate fingers in the ESD protection circuit to perform npn bipolar operations uniformly.

[36] The present invention discharges an ESD pulse effectively by forming additional or auxiliary n+ (or p+) type active regions between respective active regions. These additional active regions are connected to Vcc (or Vss).

[37] Accordingly, the present invention provides a pair of gates in a single active region for designing an NMOS type ESD protection circuit unit. By connecting the NMOS type ESD protection circuit units in parallel each other and by keeping uniform parasitic npn bipolar operations between the respective drains and sources, the present invention provides an ESD protection circuit/device having ESD characteristic that is more excellent than that of the related art.

[38] Furthermore, the present invention provides n+ (or p+) junctions, which are connected to Vcc(or Vss), additionally between respective active regions each of

which includes a limited number of gates (e.g., two gates). Accordingly, the present invention effectively discharges a positive ESD pulse by a parasitic npn bipolar operation occurring between the n+ junctions of the drain region connected to the pad and the additionally-formed active region.

[39] The present invention effectively discharges a negative ESD pulse by a parasitic np diode operation occurring between the n+ junction of the drain region connected to the pad and the p+ junction of the additionally-formed active region.

[40] The forgoing embodiments are merely exemplary and are not to be construed as limiting the present invention. The present teachings can be readily applied to other types of apparatuses, devices or, systems, or any other applicable mediums. The description of the present invention is intended to be illustrative, and not to limit the scope of the claims. Many alternatives, modifications, and variations will be apparent to those skilled in the

art.